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BEHAVIORAL COMPUTER MODEL OF TOPSWITCH

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Abstract: *A behavioral SPICE model of TOPSwitch is developed in the paper. Computer realization of the parameterized model corresponding to the functional description of the TOPSwich is proposed. The parameterized PSpice macromodel is created in the form of block in schematic view. The minimal energy levels of self-start and break of the work of TOPSwitch are presented with logical functions and Schmitt triggers. The vaweforms representing the characteristics of TOPSwitch are given.*

Key Words: ***Spice simulation, Model, Power Supply, SMPS, TOPSwitch***

1. INTRODUCTION

The process of increasing the complexity of electronic devices needs computer simulation and testing the non-faulty work by any conditions. This is expressed in the great extend in the design process of electronic units providing power supply to the electronic equipment. Complicated mathematical models are used to describe the functional behavior of complex networks. The model complication leads to a continuous need to increase the computer speed and memory resources in the simulation process. Typical examples of such models are the models of management units in SMPS (Switch Module Power Supply). Due to the high complexity, they are distributed in relatively simple structures of control chips. The processing of feedback information, the control of the pulse width modulation in starting, normal and critical modes of operation, are integrated in the more complex control structures such as TOPSwitch. Typical examples are the elements of the series TOPSwitch company Power Integrations. The simplified internal structure of TOPSwitch is presented in Fig. 1.

In the present paper a relatively simple and sufficiently effective mathematical behavioral model of the TOPSwitch is developed. It describes the basic performance features of the integrated circuit.

The simplified functional structure of TOPSwitch is shown in Fig. 2. The basic element in this structure is the functional converter $I_C \rightarrow$ PWM.

A SPICE model is constructed, corresponding to this structure. The basic functional dependencies of the TOPSwitch control are considered. A computer realization of the parameterized model corresponding to the functional description of the TOPSwitch control is performed. The minimal energy levels of self-start and break of the work of TOPSwitch are presented with logical functions and Schmitt triggers. Based on the functional dependencies of the TOPSwitch, a simplified and effective behavioral *SPICE* model of TOPSwitch is developed. The parameterized *PSpice* macromodel is created in the form of block in schematic view. The waveforms representing the characteristics of TOPSwitch are given.

The basic idea of the control structure of TopSwitch is that the control of the duty cycle of the pulse width modulation of the chip is realized by monitoring the current generated by the feedback displaced of the start and stop voltage levels as shown in Fig. 3. The dependence of the charge on the control element voltage during the startup process and normal operation is presented in Fig. 4. It demonstrates the need of a minimal energy level of the feedback in connection with the process of standby and normal TOPSwitch operation. A *PSpice* description of the TOPSwitch during the startup process and normal operation is proposed in [3]. The dependence of the charge on the control element voltage during the startup process and the standby process where the charge is not finished, is presented in Fig. 5.

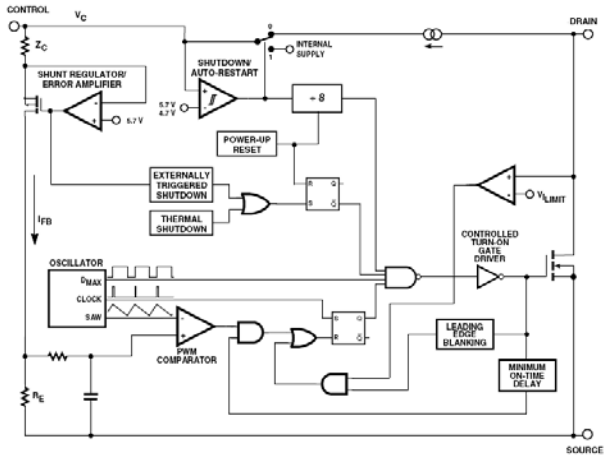


Fig. 1. *Simplified internal structure of TOPSwitch*

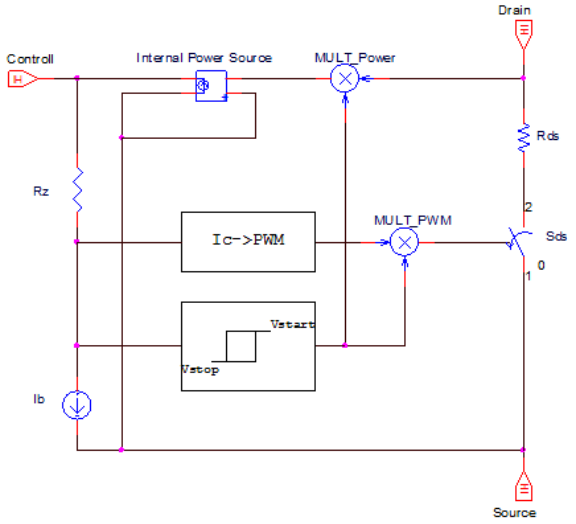


Fig. 2. *Simplified functional structure of TOPSwich*

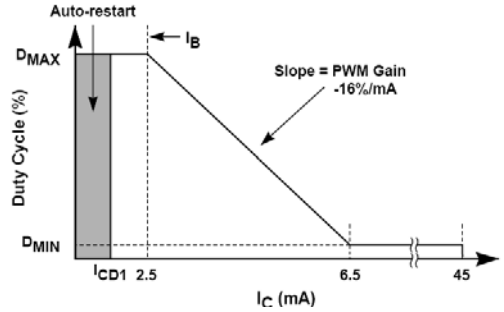


Fig. 3. *The dependence of the duty cycle on the monitoring current*

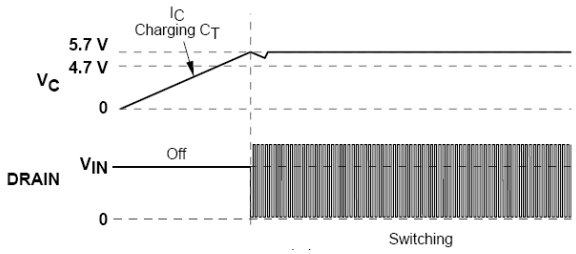


Fig. 4. *The dependence of the charge on the control element voltage during the startup process and normal operation*

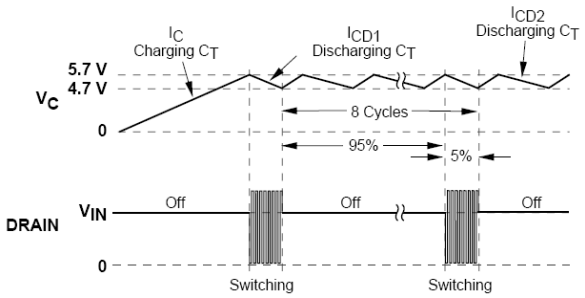


Fig. 5. *The dependence of the charge on the control element voltage during the startup process and standby where the charge is not finished*

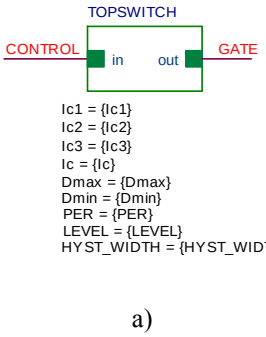
2. DESCRIPTION OF THE BEHAVIORAL COMPUTER MODEL

The dependence of the duty cycle $D_c(t)$ on the monitoring current $I_c(t)$ (Fig. 3) has the form:

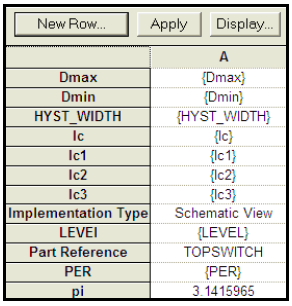
$$D_c(t)=\begin{cases} D_{\max} & for \quad i_c(t) \le I_{c1} \\ D_{max}\dfrac{i_c(t)-I_{c2}}{I_{c1}-I_{c2}} & for\ I_{c1} < i_c(t) < I_{c2} \\ D_{\min} & for\ I_{c2} \le i_c(t) < I_{c3} \\ 0 & for\ i_c \ge I_{c3} \end{cases} \quad (1)$$

The block representing the behavioral TOPSwitch *PSpice* model is shown in Fig. 6a. The parameter values of the behavioral model are defined by the pseudo-component PARAMETERS. They are translated in the circuit file using .PARAM statement in the form:

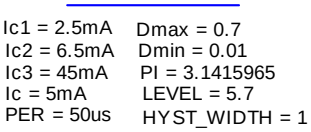
.PARAM Ic1=2.5mA, Ic2=6.5mA, PER=50us,
+ Ic3=45mA, Ic=5mA, pi=3.1415965, LEVEL=5.7,
+ HYST_WIDTH=1, Dmin=0.01, Dmax=0.7



a)



b)



c)

Fig. 6. *Block definition of the behavioral TOPSwitch model*

The parameters I_{c1}, I_{c2}, I_{c3}, I_c, D_c, D_{max}, D_{min} (Fig. 3), *PER*, *LEVEL* and *HYST_WIDTH* are defined as attributes in the *Property* menu of the block (Fig. 6b). The parameters *LEVEL* and *HYST_WIDTH* are in the form:

$$LEVEL = V_{c1}, \quad (2)$$

$$HYST\_WIDTH = V_{c1} - V_{c2}, \quad (3)$$

where V_{c1} = 5.7V , V_{c2} = 4.7V (Fig. 4).

The pulse width is:

$$PW(t) = PER.\ D_c(t) \quad (4)$$

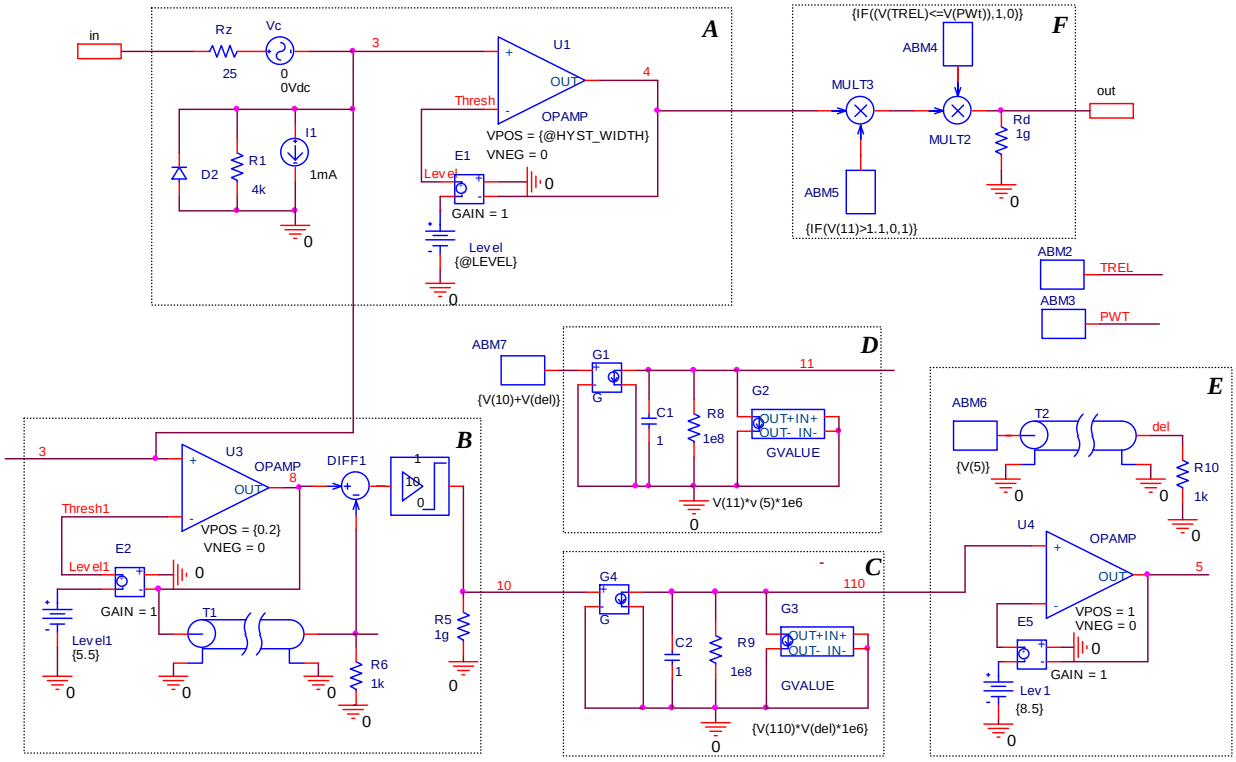


Fig. 7. *Behavioral TOPSwitch model*

The behavioral model of the TOPSwitch is represented in Fig. 7. Using the element of *ABM* type, a signal *V*(*TREL*) is created of value, equal to the time interval *TREL* from the beginning of the current rectangle pulse. The function *mod*(*a*,*b*) is used to obtain *TREL*, which returns the remainder when *a* is divided by *b* [4]:

$$\mathrm{mod}(a,b) = \frac{b}{\pi}\left(\arctan\left(\tan\left(\frac{a}{b}\pi - \frac{\pi}{2}\right)\right) + \frac{\pi}{2}\right). \qquad (5)$$

TREL and *PW*(*t*) are represented with the signals *V*(*TREL*) and *V*(*PWT*) of the elements *ABM2* and *ABM3* in the model.

The description in the *Property* menu of the element *ABM2* for the time interval *TREL* is:

```
EXPR1={(@PER)*(atan(tan(((TIME)/(@PER))*
      @pi-@pi/2))+@pi/2)/@pi}
```

The pulse width *PW*(*t*) (4) is defined in the form:

```
EXPR1= {@PER*IF((I(Vc)<=@Ic1),@Dmax,
      IF((I(Vc)>=@Ic2),@Dmin,@Dmax*
      (I(Vc)-@Ic2)/(@Ic1-@Ic2)))}
```

The IF-THEN-ELSE function is used for calculation of the duty cicle $D_c = f(I_c)$ according to Fig. 3 and (1).

The block *A* shown in Fig. 7 creates the enable function V(4) for the pulse width modulated signal (Fig. 9).The signal V(4) = 1 when the increasing control signal V_c reaches the upper level V_{c1} and V(4) = 0 when the decreasing control signal V(3) reaches the lower level V_{c2}.

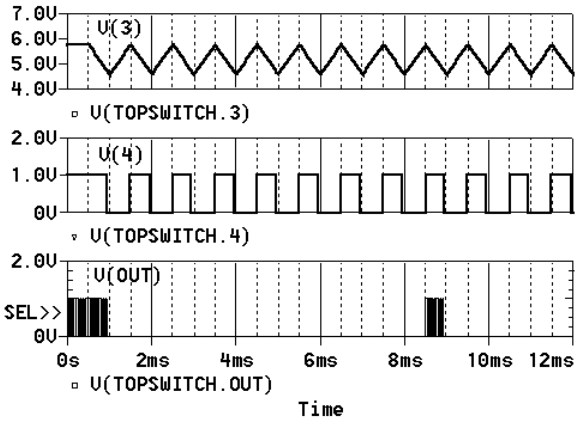


Fig. 9. *Enable signal V(4) and output signal V(out)*

During the startup process and normal operation and after the standby interval, pulse width modulated signal V(out) is generated when V(4) = 1 as shown in Fig. 9. The block *A* is realised using a Schmitt trigger.

The block *B* shown in Fig. 7 creates rectangle pulses V(10) of equal width (Fig. 10c). The pulse width is defined by the delay element T1. The signal V(10) is created from the control signal using a Schmitt trigger. Its output signal V(8) and the delayed output signal V(9) are substracted by the block DIFF1 in order to obtain V(10).

According to Fig. 5, the standby process ends after 8 discharge cycles. The signal V(10) during the standby is integrated in block *C*. The obtained integrated signal is V(110) (Fig. 11d).

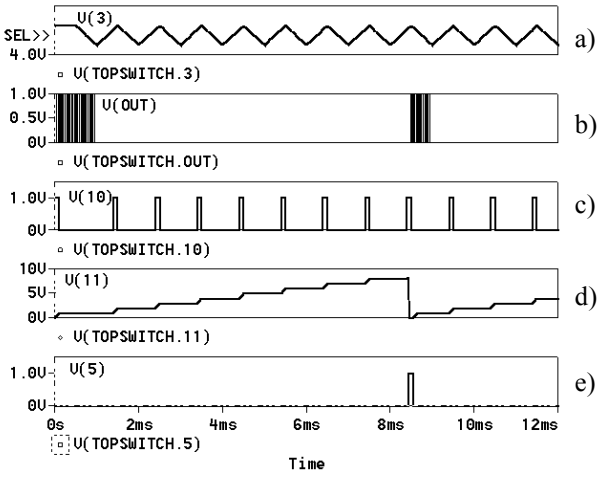


Fig. 10. *Waveforms of the generated signals in the behavior TOPSwitch model*

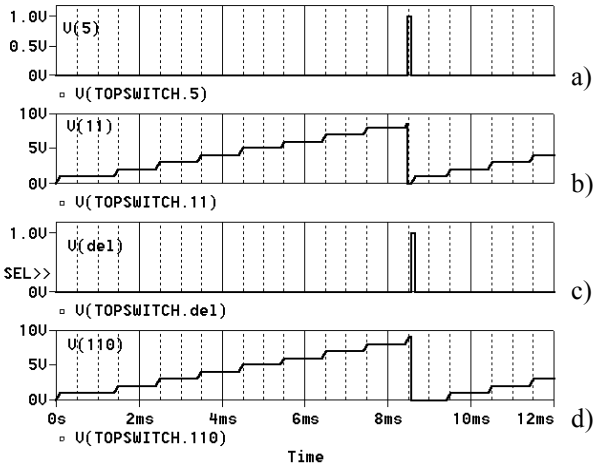


Fig. 11. *Output signals of the integrator blocks C and D and control pulses V(5) and V(del)*

The voltage controlled current source (VCCS) G3 is equivalent to a voltage controlled switch. It is used to discharge the capacitor C2 after 8 discharge cycles.

The control voltage of the VCCS G3 is the pulse V(del) shown in Fig. 11. It is created in block *E* by a Schmitt trigger and a delay element.

In order to create the pulse modilated signal in the last discharge cycle as shown in Fig. 10, the signal V(5) is delayed and added to the signal V(10) in the block ABM7. The block *D* is used to integrate the signal {V(10)+V(del)}. In this way, after 8 discharge cycles the integrated signal V(11) starts from 1 (Fig. 11b) thus enabling the pulse width modulated signal V(out). The control voltage of G2 is the pulse V(5) discharging the capacitor C1. The output signals V(110) and V(11) of the integrator blocks *C* and *D*, together with the control pulses V(del and V(5), are presented in Fig. 11.

The pulse width modulated signal is created using ABM element ABM4 in block *F* (Fig. 7). The pulses are defined by the expression:

{IF((V(TREL)<=V(PWT)),1,0)}

The element ABM5 in block F is used to disallow the pulse width modulated signal during the standby process. Its functional description is in the form:

{IF(V(11)>1.1,0,1)}.

The developed behavioral TOPSwitch model is easy for the use by designers for computer simulation of complex networks. The parameterisation makes the model universal and flexible.

The usage the VCCS G2 and G3 instead voltage controlled switches of SBreak type ensures a stable work of the model during the time-domain simulation without a loss of convergency.

3. CONCLUSION

A simplified and effective behavioral SPICE model of TOPSwitch has been developed. The basic functional dependencies of the TOPSwitch control are considered. The computer parameterized *PSpice* macromodel is created using a block in schematic view. The vaweforms representing the characteristics of TOPSwitch are given.

4. ACKNOWLEDGEMENT

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5. REFERENCES

[1] *Power Integrations – HandBook and Manual Design*, NJ 2003

[2] http://www.powerint.com/en/forum/ powersupplydesign/ top258

[3] D. Todorov, E. Gadjeva, G. Kunov, *Simplified SPICE Model of TOPSWICH*, XLIV International Scientific Conference, Information, Communication and Energy Systems and Technologies (ICEST) 25-27 June, 2009, Veliko Tarnovo, BULGARIA, vol. 1, pp. 523-526.

[4] *MicroSim Application Notes*, appnts.pdf, 1997.

[5] *PSpice User's Guide*, Cadence Design Systems, 2003.